Digital Modular Control of High Frequency DC-DC Converters

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***Abstract*— This paper presents a solution for controlling integrated DC-DC converters with switching frequency above 20 MHz. The increase of the switching frequency is a trend biased by output filter volume restrictions and integration demand. The control of DC-DC converters operating at high frequency presents an opportunity to speed up the converter response time but also a challenge specially to limit the sensitivity to process and operating conditions for the mixed signal circuits involved. The solution presented in this work relies on separating the duty-cycle into three parts: an OP load-free value that depends only on the input and output voltages, a transient fast correction contribution, and an accurate compensation for the IR drop that depends on the load current. The duty-cycle is obtained with these contributions in two digitally controlled delays. The OP portion of the delay has a compensation of PVT variations and the fast transient part of the duty-cycle uses a non-linear sliding mode control solution.**

Keywords – DC-DC converter, digital control, sliding mode control, process temperature and suply variation (PVT)

I. INTRODUCTION

Integrated DC-DC converters are now present in almost all consumer electronics due to the need of high efficiency in power supplies. On portable equipment, where the presence of DC-DC converters is stronger due to their efficiency impact on the autonomy, volume is an important figure of merit, contributing to solutions where DC-DC converters are integrated in Systems-on-Chip (SoC) and the volume of the output filter is progressively being reduced. In recent years, with the growing presence of portable, DC-DCs have been pushed to crescent switching frequencies in order to allow the desired output filter volume reduction. Currently a typical SoC includes DC-DC converters supplied by lithium batteries and switching below 5 MHz These are required to deliver 100 mA to 3 A @<1.2V, depending on the application. But there is also a trend to place DC-DC converters on SoC solutions where previously only linear regulators where used like smart cards and security chips. In this cases the full DC-DC including the output filter needs to be integrated into the SoC and the power requirements for the cryptography machines and flash and communication controllers is 20 mA to 150 mA @<1.2V. For these cases a much higher switching frequencies are required and one of the main challenges is the control implementation.

Analog control solutions that limit the duty-cycle based on real time decision of comparators are not suitable since the comparators response time is longer than the period of switching for high frequency DC-DCs. Faster comparators could be designed but it would impact severely the efficiency due to the higher current consumption.

Purely analog solutions using voltage to delay conversion can be found in [1] and [2]. However, [1] focuses only the efficiency and does not evaluate the control solution used. In [2] a DC-DC converter was designed and operates at 120 MHz with peak efficiency of 87% at 500mA using a 36nH inductor and a 4.7uF capacitor in the output filter. However, the impact of process, voltage and temperature (PVT) variations in the analog voltage to pulse converter and stability are not analyzed and the slow control speed results into a large output capacitor needed to accommodate the load transients. The major limitation of the solutions proposed in [1] and [2] is the fact that the duty-cycle consists in a unique delay controlled by a current, i. The delay depends on 1/i and, therefore, the transient response is strongly dependent on the operating point dictated by the bias operating point ($D_{OP} = V_O/V_I + D_{IRlosses}$). This work proposes to add this D_{OP} with a digitally controlled number of additional delays for transient response optimization.

Many digital control solutions have been proposed for the control of DC-DCs. The Proximate Time-Optimal Digital Control (PTODC) [3] combines a linear controller and a Non-Linear controller. Han Wei and Meng Tong Tan [4] use V2 with reduction of steady-state oscillations. [5] presents a Hybrid Digital Pulse Width Modulator (DPWM) with a frequency domain ADC. A Dual-Band Switching Digital Controller was suggested by [6]. An Autotuning Digitally Controlled Buck converter [7] based on relay feedback uses iterative procedures to obtain the PID parameters. A model -free control with "intelligent" PI controllers is proposed in [8]. The "Digital Load Current Feed-Forward Control" [9] uses a PID controller and feed-forward duty-cycle from the capacitor charge, calculated from the inductor current. The "Fully-Digital Hysteretic Voltage Mode Control" based on Asynchronous Sampling [10] uses the output voltage and the control state to estimate the inductor current. A PWM PID digital control is proposed in [11]. A Simple Non-linear gain Scheduling [12] method in Digital PWM Converter uses the last three samples of the output voltage, and the last duty cycle

value, to control the buck converter. A previous description of a Digital Sliding Mode Control (SMC) for a DC-DC can be found in [13]. It uses a voltage to frequency converter to convert the output voltage into a variable frequency square wave. The steady state is achieved by doing the difference, in the frequency domain, between the signal generated by the reference voltage and the converted output voltage. In steady state, a delay line and a counter are used to generate the DC-DC control signal. The work presents an original digital implementation of the SMC with a self-adaptive ADC. The proposed control presents stable frequency of operation and very high performance for line and load transients for 600 kHz switching frequency.

The use of the Sliding Mode Control to control a DC-DC converter has the advantage of being a robust control approach. Most implementations of the Sliding Mode Control of DC-DCs are analog implementations. Several authors implemented the Sliding Mode Control directly [14] [15] [16], while others used the equivalent control law obtained from the Sliding Mode Control [17] [18]. The major drawback of analog implementations of the sliding mode control for integrated DC-DCs, operating in the few Mega Hertz range, is the bandwidth required for the amplifier that implements the required control law. The implementation of suitable bandwidth amplifiers is not feasible for high frequency DC-DCs.

Digital control solutions frequently require frequencies of operation higher than the switching frequency in order to compute the duty-cycle value in real time. However, for high switching frequency, the power consumption of digital control, that requires even higher control frequency, severely impacts the DC-DC efficiency specially when operating at light loads. Moreover, the power required for the digital control operation must be added to the power required for the analog to digital conversion of the output voltage. Therefore, non-linear analog-to-digital conversion with a very limited number of quantization ranges is fundamental in order to allow fast feedback with limited power being wasted in this quantification.

In this work, a digital control solution is presented for high frequency DC-DC converters that implements a non-linear sliding mode control only requiring the quantification of the output voltage in three ranges (two comparators) and knowing the output voltage derivative (by comparing two consecutive samples).

The rest of the paper is organized as follows: section II presents the proposed control methodology; the implementation is detailed in section III; section VI presents simulation results and the conclusions of this work are summarized in section V.

II. MODULAR CONTROL ARCHITECTURE

Fig 1 presents the block diagram of a DC-DC buck converter, detailing the transistors that implement the power switches and the output filter.

When using constant frequency of operation (most of the times in order to limit the noise spectrum), the purpose of the controller is to define the duty-cycle of the PWM signal and therefore, the energy transferred to the output filter. This duty-cycle has three distinct contributions:

- D_{ideal} – corresponds to the ideal duty-cycle of a converter without resistive losses and working in steady state.
- $D_{IRlosses}$ – represents the increment in the duty-cycle required in order to compensate de resistive losses.
- d – is a temporary addition or subtraction to the duty-cycle that enables the dynamic correction of the output voltage during line or load transients.

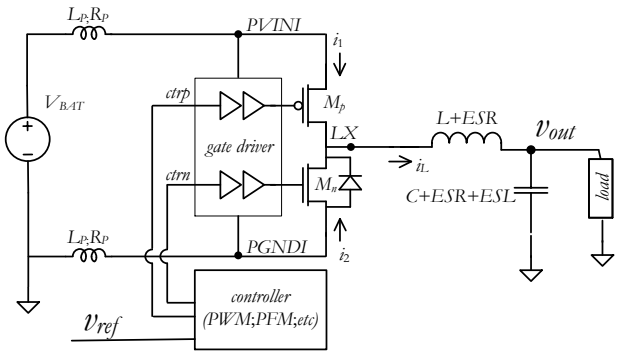

Fig 1 – DC-DC buck converter.

The sum of the first two contributions is defined as the operating point duty-cycle ($D_{OP} = D_{ideal} + D_{IRlosses}$) and corresponds to the steady state duty-cycle for specific values of v_{out}, v_{BAT} and i_L.

The variation limits and the dynamics required for each contribution to the duty-cycle is distinct and the ability to optimize them individually is a major advantage of this modular control approach. D_{ideal} and d usually require a large range of variation while $D_{IRlosses}$ consists in very limited adjustments to the duty-cycle. The variables that dynamically can be used to optimize each contribution are different: D_{ideal} depends only on the input and target output voltages. As defined in (1).

$$D_{ideal} = v_{ref}/v_{BAT} \quad (1)$$

In order to evaluate which variables are relevant for the optimization of $D_{IRlosses}$ it is required to analyze the required change in the duty-cycle, $\Delta D_{IRlosses}$, that can compensate an increase of load current from $i_L=I$ to $i_L=I+\Delta i$. Considering that i_L flows through R, that represents all the resistive losses, it can be easily obtained that:

$$\Delta D_{IRlosses} = (2+ \Delta i/I) \times \Delta i \times R / v_{BAT} \quad (2)$$

Equations (1) and (2) allow the conclusion that an increase in the input voltage causes the obvious reduction of the D_{ideal}, but, in the presence of a load change, $D_{IRlosses}$ is optimally adapted if it also varies proportionally to $1/ v_{BAT}$. If a mechanism is implemented to adjust D_{ideal}, the required similar dependence of $D_{IRlosses}$ on the supply voltage can be implemented in the

control by making the digitally controlled increments in $D_{IRlosses}$ proportional to D_{ideal}.

The *d* contribution for the duty cycle, being the correction factor for transient variations of the output voltage, can be adjusted taking into account the output voltage value and its derivative using sliding mode control.

Using a modular and digital control it is possible to optimize the dynamics of each contribution.

III. Modular Digital Control Implementation

When designing a control for high frequency of operation one of the major challenges is dealing with the parametric variations due to process, supply voltage and temperature (PVT). In fact, since the delays to control are much shorter, these variations produce much more significant relative impact. Therefore, it is mandatory to use solutions that compensate PVT and are able to produce the expected delays for the control.

The solution used in this work to obtain D_{ideal} is presented in Fig. 2 and consists in a delay locked loop working at a fixed frequency, $f = 1/T$, controlled in current, and forced to produce a control voltage of:

$$v_{ref} = D_{ideal} \times v_{BAT} \quad (3)$$

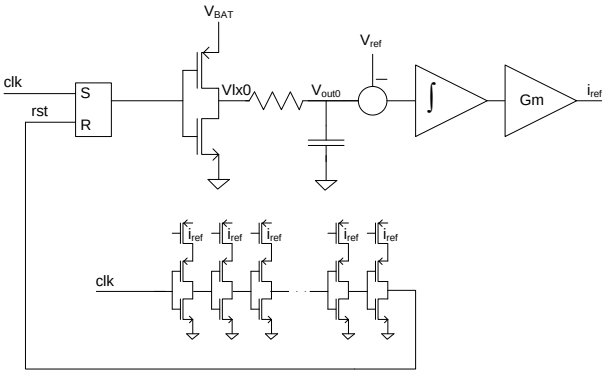

Fig 2 – DLL for the generation of i_{ctr} and $T \times D_{ideal}$.

This DLL implements two tasks:

- Forces a current controlled delay line to present a constant a delay, $T \times D_{ideal}$
- Generates a current, i_{ctr}, that when used in cells similar to the ones used in the delay line, produces a delay proportional to $1/ v_{BAT}$ and is independent of PVT variations.

Fig. 3 shows how the duty-cycle contribution for the required action during transients, *d*, is obtained: using a multiplexer, digitally controlled that adds or removes delays from the delay line of the DLL. The decision is taken based on the information of three comparators:

- One comparator compares the sampled output voltage with the value of the previous clock cycle – provides the derivative of the output voltage
- Two comparators create a hysteresis window of 20mV centered in v_{ref}.

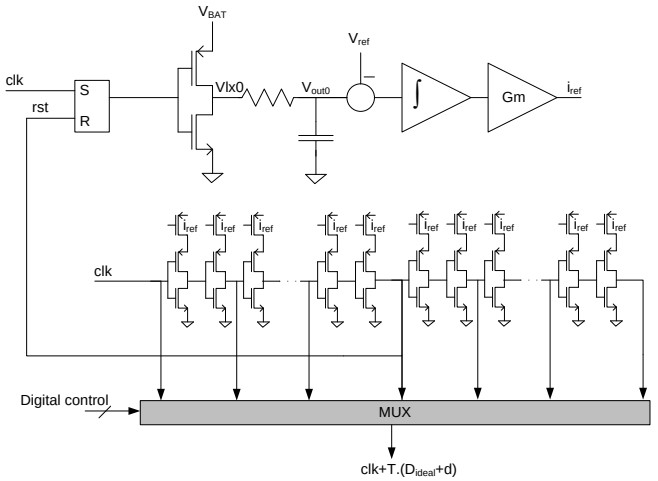

Fig 3 – DLL for the generation of $T \times (D_{ideal}+d)$.

Fig. 4 shows the Delay Locked Loop (DLL) generating a constant duty-cycle for different PVT values in an AMS

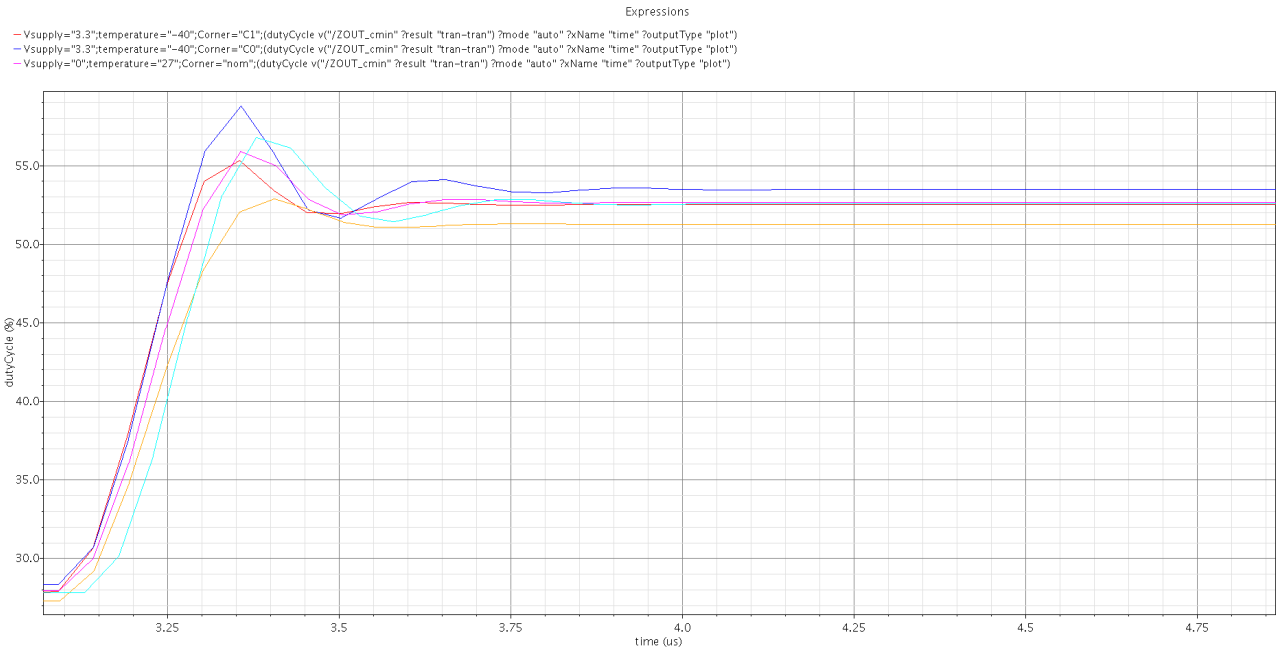

Fig. 4 – Duty-cycle obtained with PVT variation in AMS 0.35um with the topology of Fig. 2

0.35um implementation. The presented duty-cycle value corresponds to the duty-cycle of node Vlx0 of Fig. 2 and therefore is D_{ideal}.

Based on the information of these three comparators a non linear sliding mode control is implemented as follows. When the output voltage is above v_{ref} more than 10mV and the derivative is positive, *d* is reduced *1* step in the first occurrence and 3^{n-1} streps in the following occurrence *n*. *d* is reset to the original position at the exact cycle when the derivative changes sign.

Fig. 5 shows how the generation of $D_{IRlosses}$ is obtained. Since the delays required for an effective control with the required accuracy, in this contribution for the duty-cycle, need to be very small, a solution was used that consists of using PMOS transistors as capacitances that are digitally turned on or off. The gates of all transistors are connected to the capacitance node of the delay element. When the digital control wants to connect the corresponding capacitance forces the supply voltage in the drain and source. Since the current that limits each delay stage is i_{ctr}, controlled by the DLL, this delay is proportional to $1/\ v_{BAT}$ which is the appropriate dependence as shown in section II.

The control of this contribution to the duty-cycle is made synchronized with the correction required for transients (*d*). For each clock cycle that the control of *d* is acting in the DLL delay line, it also acts adding or removing capacitance to control the $D_{IRlosses}$. However, when the control of *d* does a reset due to a derivative inversion, the value accumulated in $D_{IRlosses}$ remains as is.

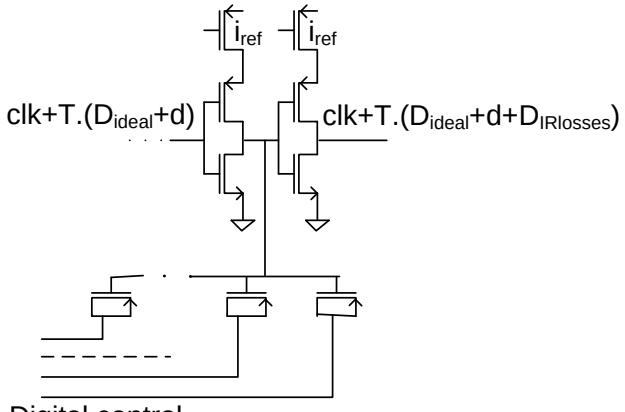

Fig 5 – Delay line for generation of $T \times (D_{ideal}+d+ D_{IRlosses})$.

IV. Simulation Results

The proposed control method was simulated using a model of a DC-DC converter with frequency of operation 20MHz, an inductor of 80nH with an ESR of 5.4mΩ. The output capacitor has 10uF an ESR of 20mΩ and an ESL of 0.22nH.

Fig. 6 presents a line transient when the input voltage changes from 3V to 4.2V. In this line transient a significant change in the duty-cycle is noticed but the output voltage changes less than 20mV.

Figures 7 ad 8 present a load transient when the output current changes from 100mA to 1.1A. Once again, very significant change in the duty-cycle, in this case only during the transient, but with limited impact on the output voltage. The load transient is very fast: approximately half a microsecond.

Fig. 8 shows clearly the action of the proposed modular control approach: when the load transient occurs, the duty-cycle is increased with growing steps until the output voltage derivative changes and, when it does, the *d* contribution is removed but the increase in $D_{IRlosses}$ made during the transient remains and the figure shows that the estimated value for this contribution is correct since the duty-cycle achieves its final steady state value for this load.

V. Conclusions

The present work shows that it is possible to split the duty-cycle components of a DC-DC converter and digitally control the delays responsible for each part, with the appropriate accuracy and speed. This modular solution is tolerant to PVT variations and is suitable for the control of high frequency DC-DC converters. A DLL, with forced frequency and forced feedback voltage, generates a current that controls all the delays that contribute to the duty-cycle. With this approach the desired proportionality to $1/\ v_{BAT}$ is obtained. Different delay elements are used for the different contributions for the duty-cycle. The transient compensation and the ideal duty-cycle ($D_{ideal}+d$) are obtained with current starving inverters acting as delay cells. The higher resolution in the delay required by the $D_{Irlosses}$ is obtained by digitally adding or removing capacitors implemented by MOS transistors. The proposed control method proved to provide fast load transients and at the same time that correctly predicts the increment required in the duty-cycle in order to compensate IR losses.

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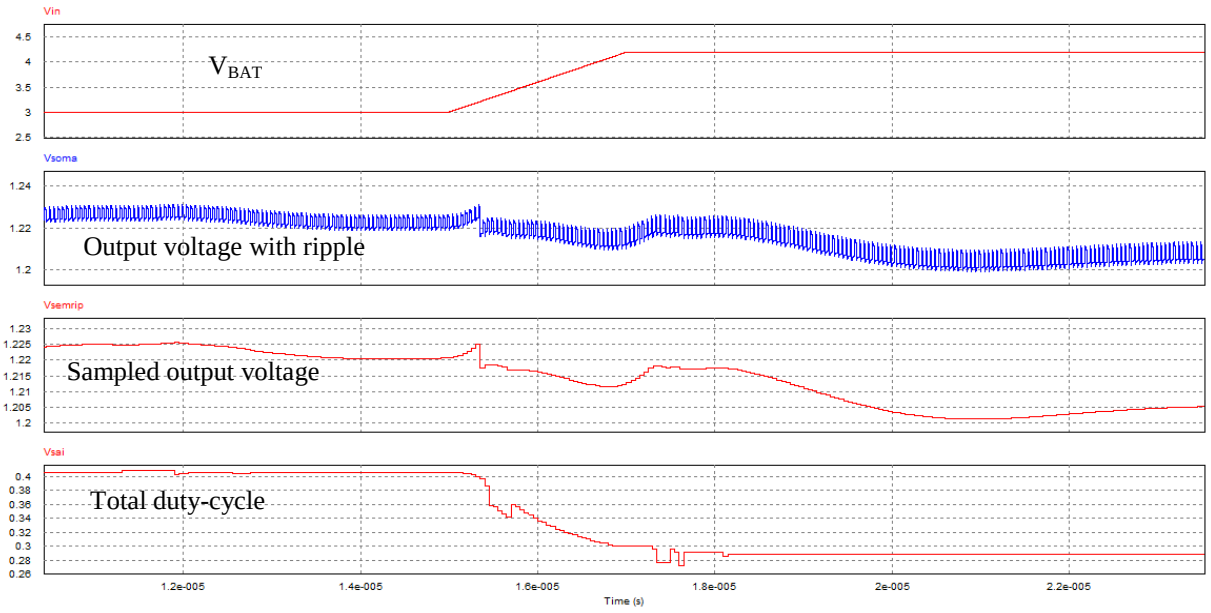

Fig. 6 – Line transient.

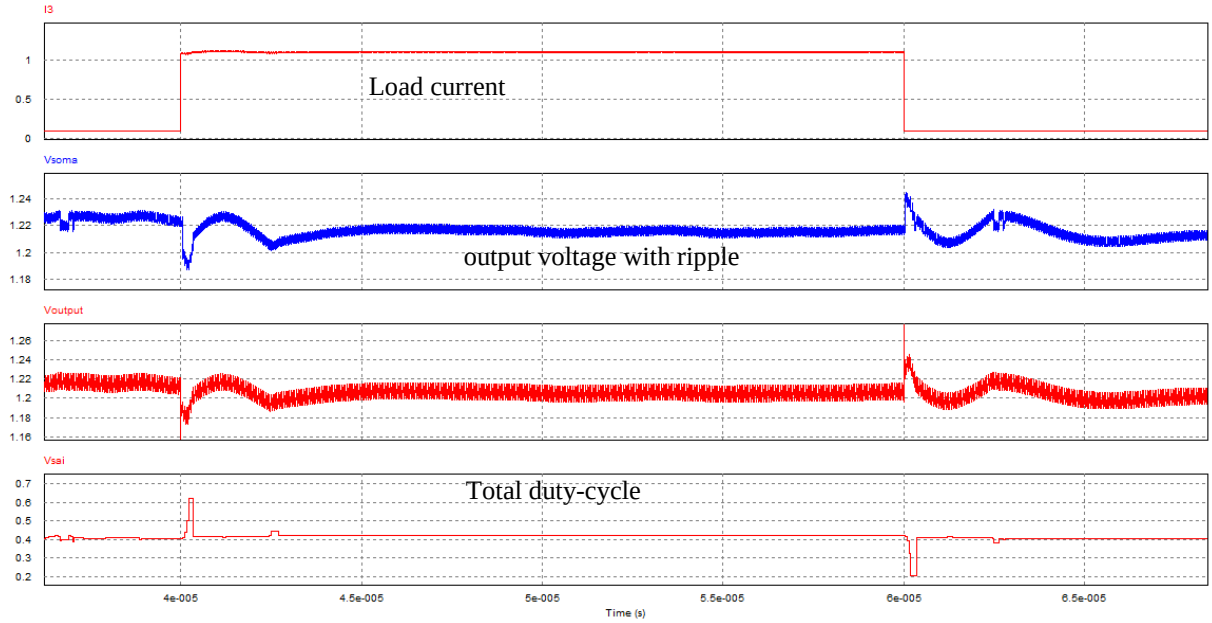

Fig. 7 – Load transient.

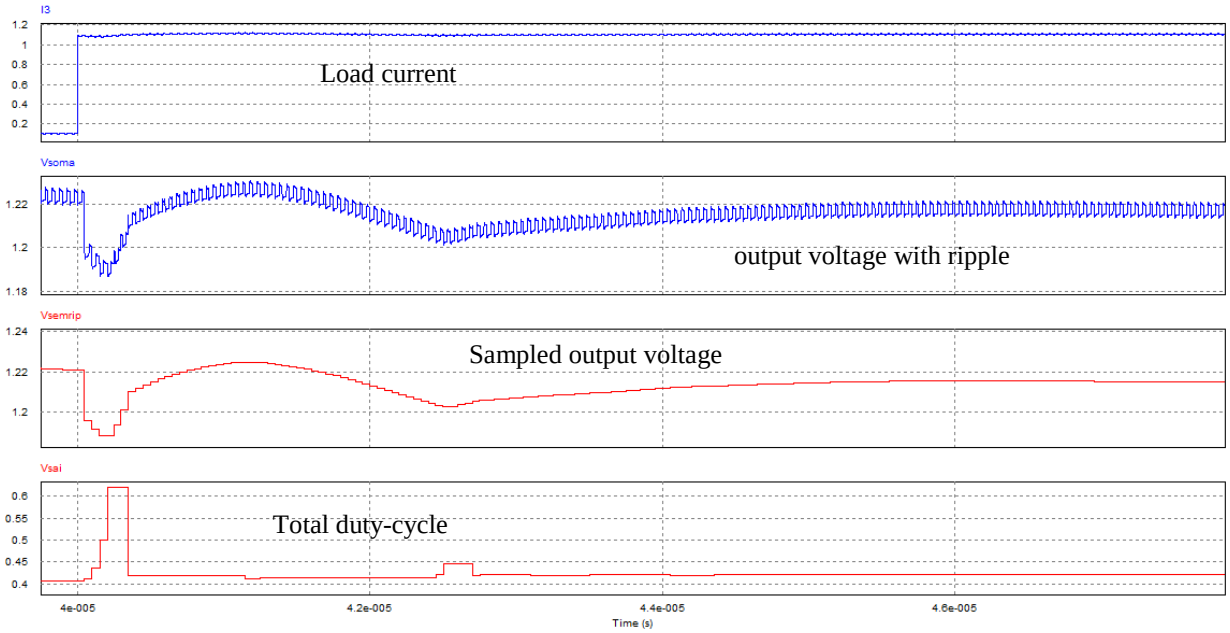

Fig. 8 – Load transient detail.